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(54) CMOS pixel using vertical structure and sub-micron CMOS process

(57) A CMOS pixel responsive to different colors of optical radiation without the use of color filters is described. A deep N well is formed in a P type silicon substrate. An N well is then formed at the outer periphery of the deep N well to form a P well within an N well structure. Two N^+ regions are formed in the P well and at least one P^+ region is formed in the N well A layer of gate oxide and a polysilicon electrode is then formed over one of the N^+ regions. The PN junction between the deep N well and the P type silicon substrate is responsive to red light. The PN junction between the deep N well and the P well is responsive to red light. The PN junction between the P well and the N^+ region which is not covered by polysilicon and the PN junction formed by the N well and the P^+ region are responsive to green or blue light. The PN junction formed by the junction between the P well and the N^+ region which is covered by polysilicon is responsive to green light. The green signal is subtracted from the blue/green signal to produce a blue signal.

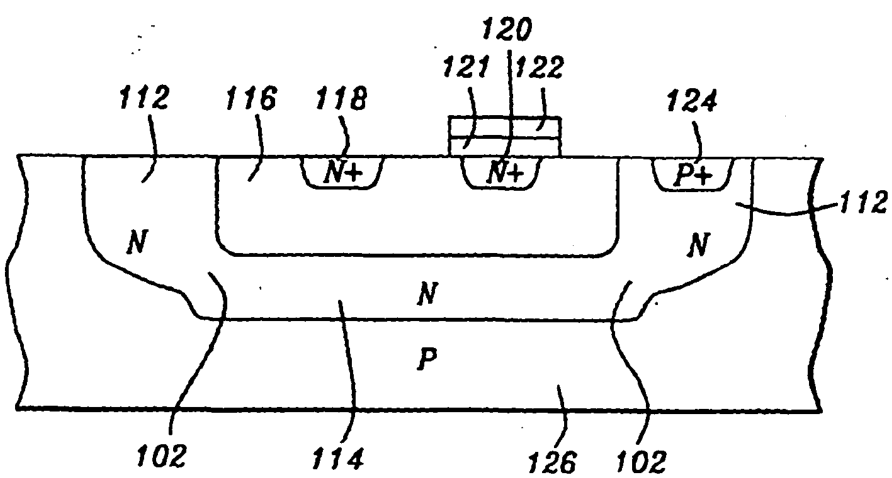

FIG. 1A

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Fig. 4 shows a schematic diagram of a circuit used to implement the pixel shown in Fig. 3.

Fig. 5 shows a cross section view of a part of the P type substrate of the pixel of Fig. 3 showing two NMOS transistors formed in the P type substrate.

Description of the preferred embodiments

[0014] Refer now to Figs. 1A-5 of the drawings for a description of the preferred embodiments of this invention. Fig. 1A shows a cross section of the vertical APS, active pixel sensor, structure of this invention. The pixel is formed in a P type epitaxial silicon substrate 126. A deep N well 114 is formed in the substrate 126 as shown in Fig. 1A. The depth of the deep N well is the same as the penetration depth for red, infrared, and deep red light in silicon and is between about 5 and 8 microns. As an example the deep N well 114 can be formed using methods such as ion implantation. An N well 112 is formed at the periphery of the deep N well 114, extending between the top surface of the substrate 126 and the deep N well, thereby forming a P well 116 within the N well 112 and above the deep N well 114. An overlap region 102 connects the deep N well 114 and the N well 112. As another example, the structure could also be formed by first forming a large N well in the substrate and a P well 116 in the large N well thereby forming the N well 112, the deep N well 114, and the overlap region 102.

[0015] A first N^+ region 118 and a second N^+ region 120 are formed in the P well 116. A P^+ region 124 is formed in the N well 112. A dielectric layer 121, such as a gate oxide, and a polysilicon layer 122 are formed over the second N^+ region and extend far enough to cover the junction between the second N^+ region 120 and the P well 116. The first N^+ region 118 and the P^+ region 124 are shallow and the PN junction between the first N^+ region 118 and the P well 116 and the PN junction between the P^+ 124 region and the N well 112 respond to blue or green light. Although the second N^+ region 120 is also shallow and has the same depth as the first N^+ region 118, the second N^+ region 120 is covered by a layer of polysilicon 122, which blocks blue light, so that the PN junction formed by the second N^+ region 120 in the P well 116 responds to green light.

[0016] Fig. 1 B shows a top view of the structure shown in Fig. 1A. Fig. 1A is a cross section view of the structure shown in Fig. 1B taken along line 1A-1A' of Fig. 1B. The periphery of the deep N well is shown as a dotted line 110 in Fig. 1B. As shown in Fig. 1B, the N well 112 has an inner periphery 109 and an outer periphery 111. Fig. 1B shows the inner periphery 109 and outer periphery 111 of the N well 112 as being essentially circular. While this example shows these peripheries to be circular, the inner periphery 109 and outer periphery 111 can have any suitable closed shape.

[0017] A schematic diagram of the pixel structure of Figs. 1A and 1B is shown in Fig. 2. In the diagram shown in Fig. 2, the combined N well/deep N well is shown as a first node 214, the P well is shown as a second node 216, the P type substrate is shown as a third node 226, the first N^+ region is shown as a fourth node 218, the second N^+ region is shown as a fifth node 220, and the P^+ region is shown as a sixth node 224. The PN junction between the combined N well/deep N well 214 and the P type substrate 226 is shown as a photodiode 236. The PN junction between the P well 216 and the combined N well/deep N well 214 is shown as a photodiode 232 and responds to red light. The PN junction between the second N^+ region 220 and the P well 216, which is covered by a layer of polysilicon, is shown as a photodiode 228 and responds to green light. The PN junction between the P^+ region 224 and the combined N well/deep N well 214 is shown as a photodiode 234 and responds to blue or green light. The PN junction between the first N^+ region 218 and the P well 216 is shown as a photodiode 238 and responds to blue or green light. Appropriate circuitry, which will presently be described, can be used to extract the red, green, and blue signals or to extract combined red/green and blue/green signals.

[0018] As those skilled in the art will recognize, this pixel can also be formed by replacing the P type substrate by an N type substrate, the first P region by a first N region, the N regions by P regions, the N^+ regions by P^+ regions, and the P^+ region by an N^+ region. This is shown in Fig. 1C showing a deep P well 114A formed in an N type epitaxial substrate 126A. A P well 112A is formed at the periphery of the deep P well 114A, extending between the top surface of the substrate 126A and the deep P well, thereby forming an N well 116A within the P well 112A and above the deep P well 114A. An overlap region 102A connects the deep P well 114A and the P well 112A. A first P^+ region 118A and a second P^+ region 120A are formed in the N well 116A. An N^+ region 124A is formed in the P well 112A. A dielectric layer 121A, such as a gate oxide, and a polysilicon layer 122A are formed over the second P^+ region and extend far enough to cover the junction between the second P^+ region 120A and the N well 116A. The first P^+ region 118A and the N^+ region 124A are shallow and the PN junction between the first P^+ region 118A and the N well 116A and the PN junction between the N^+ region 124A and the P well 112A respond to blue or green light. Although the second P^+ region 120A is also shallow and has the same depth as the first P^+ region 118A, the second P^+ region 120A is covered by a layer of polysilicon 122A, which blocks blue light, so that the PN junction formed by the second P^+ region 120A in the N well 116A responds to green light.

[0019] Figs. 3-5 show an embodiment of a circuit which can be used with the pixel shown in Figs. 1A-2. Fig. 3A shows a cross section view of the CMOS pixel shown in Figs. 1A and 1B with some additions. The pixel is formed in a P type epitaxial silicon substrate 326. A deep N well 314 is formed in the substrate 326 as shown in Fig. 1A. The depth of the deep N well 314 is the same

shown in Figs. 1A and 1B can also be used as vertical charge transfer APS, active pixel sensor. In this mode of operation the overlap region 102 is intentionally designed to be smaller. so that when the P well 116 is set to a reasonable negative bias the overlap region 102 is totally depleted even when the deep N well 114 is at its minimum potential of zero volts, thereby isolating the deep N well 114. In this mode of operation the charge depletion in the overlap region 102 is controlled by the potential of the P well 116. To reset the pixel in this operational mode the N well 112 is set to the reset voltage while the P well 116 is held at a positive voltage, so that the overlap region 102 is not depleted, and the deep N well 114 is set to the reset voltage via the overlap region 102. The P well 116 is then set to a negative voltage depleting the overlap region 102 and isolating the deep N well 114. The deep N well is then isolated and set to the reset voltage. During the charge integration cycle the potential of the deep N well 114 changes due to electron hole pairs generated by incoming light intensity. During the readout cycle the potential of the P well 116 is set to a positive voltage, the overlap region 102 is no longer depleted, and the potential of the deep N well 114 is transferred to the N well 112 where it can be read out.

[0026] This ability to deplete the overlap region 102 also allows the pixel to be used in a snapshot mode. After the potential of the deep N well 114 is transferred to the N well 112 the overlap region 102 can again be depleted so that the potential can be stored in the N well 112 until it is read out.

Claims

1. A pixel structure, comprising:

   - a substrate of a first conductivity type silicon;
   - a first well of a second conductivity type silicon formed in said substrate, wherein said first well is a distance below the top surface of said substrate, and the polarity of said second conductivity type is opposite to the polarity of said first conductivity type;
   - a second well of said second conductivity type silicon formed in said substrate, wherein the top surface of said second well is the top surface of said substrate and said second well has an inner periphery and an outer periphery;
   - an overlap region of said second conductivity type silicon between and connecting said first well and said second well;
   - a third well of said first conductivity type silicon in the region within said inner periphery of said second well and between the top surface of said substrate and said first well, wherein said first well and said second well isolate said third well from said substrate;
   - a first region of said second conductivity type silicon formed in said third well, wherein the top surface of said substrate forms the top surface of said first region;
   - a second region of said second conductivity type silicon formed in said third well, wherein the top surface of said substrate forms the top surface of said second region; and
   - a third region of said first conductivity type silicon formed in said second well, wherein the top surface of said substrate forms the top surface of said third region.

2. The pixel structure of claim 1 wherein said first conductivity type silicon is P type silicon.

3. The pixel structure of claim 1 wherein said second conductivity type is N type silicon.

4. The pixel structure of claim 1 wherein the junction between said first well and said substrate has a good response to radiation having wavelengths at or near the wavelength for red light.

5. The pixel structure of claim 1 wherein the junction between said first region and said third well and the junction between said third region and said second well have a good response to radiation having wavelengths at or near the wavelength for blue light.

6. The pixel structure of claim 1 wherein the junction between said first region and said third well and the junction between said third region and said second well are used to reset the pixel.

7. The pixel structure of claim 1, further comprising:

   - a layer of dielectric formed over said second region of said second conductivity type silicon; and
   - a layer of polysilicon formed over said layer of dielectric and covering said second region of said second conductivity type silicon.

8. The pixel structure of claim 7, wherein the junction between said second region and said third well has a good response to radiation having wavelengths at or near the wavelength for green light.

9. The pixel structure of claim 1 wherein the amount of carrier depletion in, and thereby the conductivity of, said overlap region is determined by the potential of said third well.

10. A CMOS pixel structure, comprising:

   - a substrate formed of P type epitaxial silicon;
   - a first N well, formed of N type silicon, in said substrate, wherein said first N well is a distance

23. The pixel circuit of claim 22 wherein said first NMOS transistor and said PMOS transistor are operated as source follower transistors.

24. The pixel circuit of claim 22 wherein said second NMOS transistor and said third NMOS transistor are formed in said P type substrate.

25. The pixel circuit of claim 22 wherein said third diode is formed in said N well.

26. The pixel circuit of claim 22 wherein said fourth diode is formed in said P well.

27. The pixel circuit of claim 22 wherein during the reset cycle said first reset voltage node is set at a high potential, V_{DD}, and said second reset voltage node is set at ground potential.

28. The pixel of claim 22 wherein during the charge integration cycle said first reset voltage node is set at ground potential and said second reset voltage node is set at a high potential, V_{DD}.

29. The pixel of claim 22 wherein during the readout cycle a red/green signal is taken form the drain of the third NMOS transistor.

30. The pixel of claim 22 wherein during the readout cycle a blue/green signal is taken from the source of the second NMOS transistor.

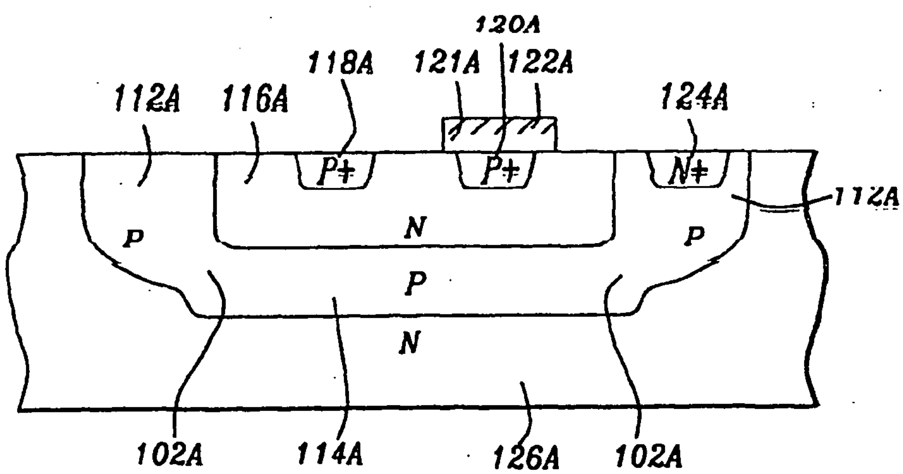
120A
118A
121A
122A
112A
116A
124A
P+
P+
N+
112A
P
N
P
P
N
102A
114A
126A
102A

FIG. 1C

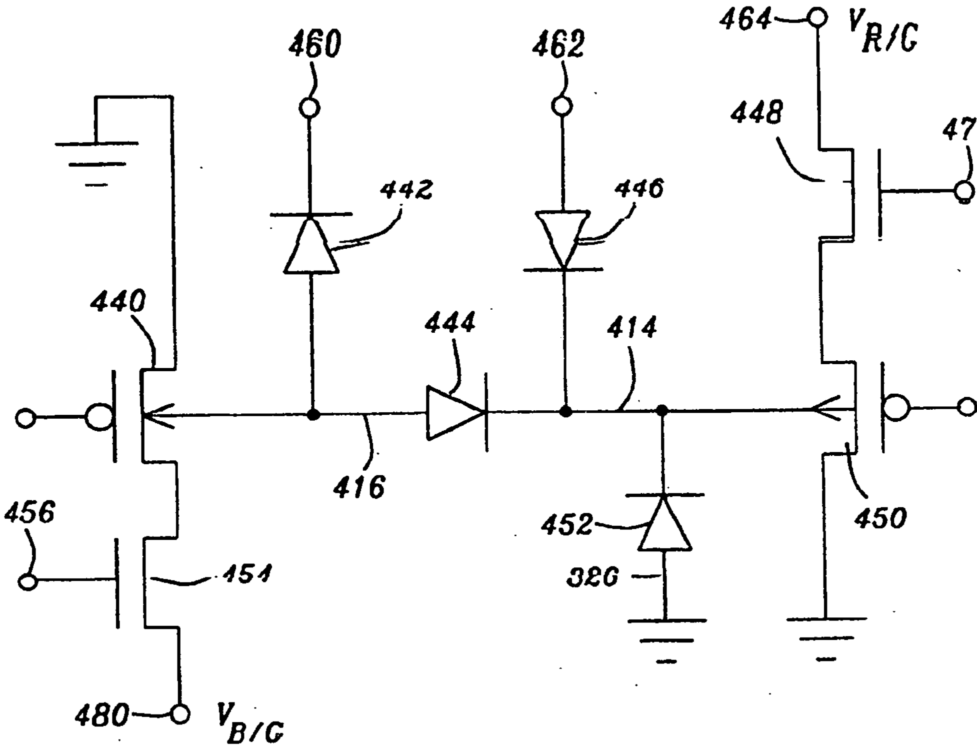
460
462
464
$V_{R/C}$
448
470
442
446
440
444
414
416
456
452
454
326
450
480
$V_{B/G}$

FIG. 4

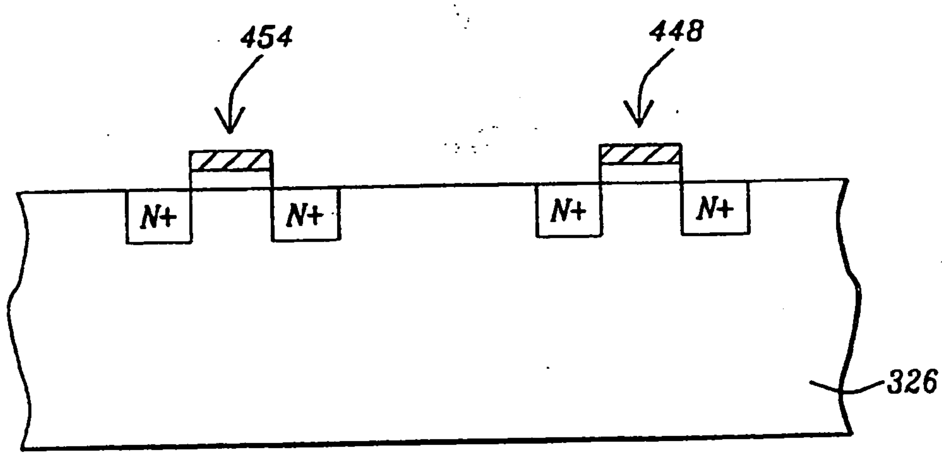
454
448
N+
N+
N+
N+
326

FIG. 5